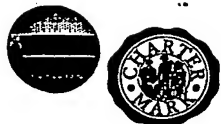
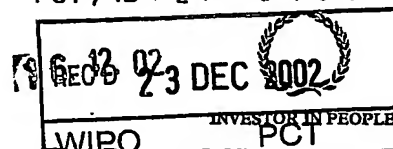


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2. Patent application number (The Patent Office will fill in this part)	0200094.1		
3. Full name, address and postcode of the or of each applicant ( <u>underline all surnames</u> )	KONINKLIJKE PHILIPS ELECTRONICS N.V. GROENEWOUDSEWEG 1 5621 BA EINDHOVEN THE NETHERLANDS		
Patents ADP Number (if you know it)	8017410001		
If the applicant is a corporate body, give the country/state of its incorporation	THE NETHERLANDS		
4. Title of the invention	BALANCED GYRATOR AND DEVICES INCLUDING THE BALANCED GYRATOR		
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# DESCRIPTION

## BALANCED GYRATOR AND DEVICES INCLUDING THE BALANCED GYRATOR

5

The present invention relates to a balanced gyrator and to devices, such as gyrator filters and integrated transceivers including at least one of the balanced gyrators.

10 Gyrator filters are frequently used in low power channel filters for wireless transceivers. Currently there is an interest in being able to fabricate complete integrated transceivers/receivers in MOS technology. Channel filters may comprise MOS gyrators which suffer from capacitive feedforward which is the result of non-reciprocal gate-drain capacitance in its MOSTs and this  
15 results in filters with a distorted high frequency response. Gyrators comprise transconductor feedback pairs and ideally transconductors linearly convert an input voltage into an output current with both input and output ports presenting an infinite impedance. A typical transconductor feedback pair is shown in Figure 1 in which one transconductor 10 is inverting and the other  
20 transconductor 12 is non-inverting.

Figure 2 shows an embodiment of a balanced class AB transconductor which comprises two pairs of MOS transistors, each pair comprising a p-type transistor 14 and a n-type transistor 16 having their drain electrodes coupled together, their source electrodes connected to respective supply voltage lines  
25  $V_{DDA}$  and  $V_{SS}$ , their gate electrodes connected together with a common junction of each pair of gate electrodes being connected to a respective input terminal 18, 20, and their respective interconnected drain electrodes coupled to output terminals 22, 24. A common mode feedback (cmfb) circuit 26 is coupled between the input terminals 18, 20 to provide dc stability.

30 A problem with a balanced gyrator such as that shown in Figure 3 using two balanced class AB transconductors 10, 12 with the output connections of the feedback transconductor 12 crossed-over is that the capacitances



A second object of the present invention is to avoid or reduce distortion in the frequency response of a filter implemented using balanced gyrators.

According to one aspect of the present invention there is provided a balanced gyrator comprising a plurality of interconnected feedforward and feedback MOS single-ended transconductors, balanced inputs and outputs, common mode feedback means coupled respectively between the balanced inputs and outputs, and means for providing each of the transconductors with a non-reciprocal feedback capacitance for rendering reciprocal the feedthrough capacitance of the transconductor thereby neutralising the feedthrough capacitance of the gyrator.

According to a second aspect of the present invention there is provided a filter comprising at least one stage including first and second shunt capacitors and a series inductance stage, characterised in that the series inductance stage comprises first and second balanced gyrators and a shunt capacitance and in that each of the first and second gyrators comprises a plurality of interconnected feedforward and feedback MOS single-ended transconductors, balanced inputs and outputs, common mode feedback means coupled respectively between the balanced inputs and outputs, and means for providing each of the transconductors with a non-reciprocal feedback capacitance for rendering reciprocal the feedthrough capacitance of the transconductor thereby neutralising the feedthrough capacitance of the gyrator.

According to a third aspect of the present invention there is provided a transceiver having at least one channel filter, the or each channel filter comprising a plurality of balanced gyrators, each balanced gyrator including a plurality of interconnected feedforward and feedback MOS single-ended transconductors, balanced inputs and outputs, common mode feedback means coupled respectively between the balanced inputs and outputs, and means for providing each of the transconductors with a non-reciprocal feedback capacitance for rendering reciprocal the feedthrough capacitance of the transconductor thereby neutralising the feedthrough capacitance of the gyrator.

The present invention also relates to the filter and the transceiver as integrated circuits.

The present invention will now be described, by way of example, with  
5 reference to the accompanying drawings, wherein:

Figure 1 is a block schematic diagram showing a gyrator comprising a feedback pair of transconductors,

Figure 2 is a diagram of a balanced class AB transconductor comprising MOS transistor pairs and a common-mode feedback circuit,

10 Figure 3 is a block schematic diagram of a balanced gyrator block comprising two balanced transconductors as shown in Figure 2,

Figure 4 is a diagram of a MOSFET showing the various intrinsic and extrinsic capacitances between pairs of electrodes,

15 Figure 5 is a graph illustrating the intrinsic capacitances of the transistors of the transconductor in various operating regions,

Figure 6 is a schematic circuit diagram of a single ended transconductor with an added feedback circuit,

20 Figure 7 is a block schematic circuit diagram of a balanced gyrator block comprising four of the single ended transconductors shown in Figure 6 and common mode feedback stages,

Figure 8 is a block schematic diagram of a fifth order gyrator filter,

25 Figure 9 illustrates, in broken lines, the frequency response of a fifth order gyrator filter in which the gyrator feedforward capacitances are not neutralised and, in full lines, the frequency response of the fifth order gyrator filter in which the gyrator feedforward capacitances have been neutralised, and

Figure 10 is a block schematic diagram of a transceiver having a polyphase filter employing balanced gyrators made in accordance with the present invention.

30 In the drawings the same reference numerals have been used to indicate corresponding features.

As Figures 1 to 5 have already been described in the preamble of the specification they will not be described again.

Referring to Figure 6 the illustrated single ended transconductor comprises pMOS and nMOS transistors 14, 16, respectively, whose drain electrodes are connected together and whose source electrodes are connected to respective current supply rails  $V_{dda}$  and  $V_{ss}$ . The gates of these transistors are connected to a common input terminal 18.

The gate-source capacitance 30 of the pMOS transistor 14,  $C_{gsp}$ , is shown in broken lines between the gate of the transistor 14 and the supply line  $V_{dda}$ . Similarly the gate-source capacitance 32 of the nMOS transistor 16,  $C_{gsn}$ , is shown in broken lines between the gate of the transistor 16 and the supply line  $V_{ss}$ . The capacitance  $C_{dgt}$  between the interconnected drains and interconnected gates of the transistors 14, 16 is shown in broken lines.

The illustrated single ended transconductor further comprises an added feedback circuit  $C_f$ . This feedback circuit  $C_f$  comprises a source follower S, pMOS transistor 36, which is biased by a current source I, pMOS transistor 34, and driven at its gate by the voltage at the transconductor output 22. The source follower output is connected to the transconductor input 18 by a capacitor  $C_p$  formed from the oxide capacitance of a MOS transistor 38. In the illustrated embodiment the transistor 38 is a pMOS transistor and if the transistor cuts-off due to signal polarity reversal the capacitance is fairly constant because the channel is replaced by the back-gate.

In a non-illustrated embodiment a reverse connected nMOS transistor (with its gate connected to the transconductor output 22 and common source-drain connected to the input 18) could be used to make the capacitor  $C_p$ . In that case, it should be biased permanently in its triode region using the source follower  $V_{gs}$ , transistor 36.

Reverting to the embodiment as illustrated, when a signal voltage is applied to the transconductor input 18, current flows by way of the capacitance  $C_{dgt}$  to the transconductor output 22 and by way of the capacitor  $C_p$  to the source follower S which routes it harmlessly to the  $V_{ss}$  rail. So:





capacitor C4, the balanced gyrators BG3, BG4 being constructed in the same manner as the balanced gyrators BG1, BG2. As the balanced gyrators BG1 to BG4 have been described with reference to Figure 7, then in the interests of brevity they will not be described again.

5        This improvement in the frequency response is illustrated in Figure 9 in which the broken line frequency response 40 shows the effect of the feedthrough capacitors not being reciprocal, as demonstrated by equation (9) above, and the full line frequency response 42 illustrates the improvement when the capacitors are reciprocal.

10       The value of the capacitance  $C_p$  (Figure 6) may be determined empirically by simulating the filter containing balanced gyrators having single-ended transconductors of the type shown in Figure 6 together with the cmfb circuits 26 and varying the size of the transistors 38 until the desired performance is achieved.

15       Figure 10 illustrates a transceiver in which a polyphase channel filter CF in the receiver section Rx comprises a Gm-C filter based on the fifth order bandpass filter shown in Figure 8. More particularly the polyphase channel filter CF comprises two fifth order bandpass filters, one for each of the quadrature related phases, with the addition of cross branch balanced gyrators  
20       coupling corresponding capacitors, that is C1, C1; C2, C2 and so on, to create extra susceptance.

      An antenna 50 is coupled to a low noise amplifier (LNA) 52 in the receiver section Rx. An output of the LNA 52 is coupled by way of a signal divider 54 to first inputs of quadrature related mixers 56, 58. A local oscillator  
25       signal generated by a signal generator 60 is applied to a second input of the mixer 56 and, by way of a ninety degree phase shifter 62, to a second input of the mixer 58. Quadrature related outputs I, Q, respectively, from the mixers 56, 58 are applied to the polyphase channel filter CF which passes the wanted quadrature related signals to respective analogue-to-digital converters 62, 64.  
30       The digital outputs from the A-to-D converters 62, 64 are applied to a digital demodulator 66 which provides an output signal on a terminal 68.

The transmitter Tx comprises a digital modulator 70 which includes a digital-to-analogue converter (not shown) providing an analogue signal to a mixer 72 for frequency up-conversion to the required transmission frequency. A power amplifier 74 amplifies the frequency up-converted signal and supplies  
5 it to the antenna 50.

The transceiver including the channel filter CF may be fabricated as an integrated circuit using known low voltage CMOS processes.

In the present specification and claims the word "a" or "an" preceding an element does not exclude the presence of a plurality of such elements. Further,  
10 the word "comprising" does not exclude the presence of other elements or steps than those listed.

From reading the present disclosure, other modifications will be apparent to persons skilled in the art. Such modifications may involve other features which are already known in the design, manufacture and use of  
15 balanced gyrator filters and component parts therefor and which may be used instead of or in addition to features already described herein. Although claims have been formulated in this application to particular combinations of features, it should be understood that the scope of the disclosure of the present application also includes any novel feature or any novel combination of  
20 features disclosed herein either explicitly or implicitly or any generalisation thereof, whether or not it relates to the same invention as presently claimed in any claim and whether or not it mitigates any or all of the same technical problems as does the present invention. The applicants hereby give notice that new claims may be formulated to such features and/or combinations of  
25 such features during the prosecution of the present application or of any further application derived therefrom.

## CLAIMS

1. A balanced gyrator comprising a plurality of interconnected feedforward and feedback MOS single-ended transconductors, balanced inputs and outputs, common mode feedback means coupled respectively between the balanced inputs and outputs, and means for providing each of the transconductors with a non-reciprocal feedback capacitance for rendering reciprocal the feedthrough capacitance of the transconductor thereby neutralising the feedthrough capacitance of the gyrator.

2. A balanced gyrator as claimed in claim 1, wherein each of the single-ended transconductors comprises a pMOS transistor and a nMOS transistor having drain electrodes connected together, source electrodes connected to respective first and second power supply lines, gate electrodes coupled to an input, and a junction of the interconnected drain electrodes connected to an output, characterised in that the non-reciprocal feedback capacitance comprises a capacitive device coupled between the input and output.

3. A balanced gyrator as claimed in claim 2, characterised in that the capacitive device comprises a MOS transistor having its source and drain electrodes connected together and a gate electrode, in that the gate electrode is coupled to the transconductor input and in that a source follower transistor couples the interconnected source and drain electrodes to the transconductor output.

4. A balanced gyrator as claimed in claim 3, characterised in that the capacitance value of the capacitive device is related to the sum of the gate-source capacitances of the pMOS and nMOS transistors.

5. A balanced gyrator as claimed in claim 4, characterised in that the capacitance value is substantially equal to:  $\frac{2}{5}(C_{gp} + C_{gn})$ , where  $C_{gp}$  and  $C_{gn}$ , respectively are the gate-source capacitances of the pMOS and nMOS transistors.

5

6. A filter comprising at least one stage including first and second shunt capacitors and a series inductance stage, characterised in that the series inductance stage comprises first and second balanced gyrators and a shunt capacitance and in that each of the first and second gyrators comprises a plurality of interconnected feedforward and feedback MOS single-ended transconductors, balanced inputs and outputs, common mode feedback means coupled respectively between the balanced inputs and outputs, and means for providing each of the transconductors with a non-reciprocal feedback capacitance for rendering reciprocal the feedthrough capacitance of the transconductor thereby neutralising the feedthrough capacitance of the gyrator.

15

7. A transceiver having at least one channel filter, the or each channel filter comprising a plurality of balanced gyrators, each balanced gyrator including a plurality of interconnected feedforward and feedback MOS single-ended transconductors, balanced inputs and outputs, common mode feedback means coupled respectively between the balanced inputs and outputs, and means for providing each of the transconductors with a non-reciprocal feedback capacitance for rendering reciprocal the feedthrough capacitance of the transconductor thereby neutralising the feedthrough capacitance of the gyrator.

25

8. A transceiver as claimed in claim 7, wherein each of the single-ended transconductors comprises a pMOS transistor and a nMOS transistor having drain electrodes connected together, source electrodes connected to respective first and second power supply lines, gate electrodes coupled to an

30

input, and a junction of the interconnected drain electrodes connected to an output, characterised in that the non-reciprocal feedback capacitance comprises a capacitive device coupled between the input and output.

5           9. A transceiver as claimed in claim 8, characterised in that the capacitive device comprises a MOS transistor having its source and drain electrodes connected together and a gate electrode, in that the gate electrode is coupled to the transconductor input and in that a source follower transistor couples the interconnected source and drain electrodes to the transconductor  
10       output.

          10. A transceiver as claimed in claim 8, characterised in that the capacitance value of the capacitive device is related to the sum of the gate-source capacitances of the pMOS and nMOS transistors.

15           11. An integrated circuit comprising a filter as claimed in claim 6.

          12. An integrated circuit comprising a transceiver as claimed in any one of claims 7 to 10.

20           13. A balanced gyrator constructed and arranged to operate substantially as hereinbefore described with reference to and as shown in the accompanying drawings.

25           14. A filter constructed and arranged to operate substantially as hereinbefore described with reference to and as shown in the accompanying drawings.

30           15. A transceiver constructed and arranged to operate substantially as hereinbefore described with reference to and as shown in the accompanying drawings.

## ABSTRACT

**BALANCED GYRATOR AND DEVICES INCLUDING THE BALANCED  
GYRATOR**

5

A balanced gyrator comprises interconnected pairs of single-ended inverting class AB transconductors (TC1 to TC4) fabricated from MOSFETs together with common mode feedback circuits (26) connected between balanced inputs (18,19) and outputs (22, 23). Peaking of the filter's frequency response resulting from distortion due to the creation of a high frequency parasitic feedthrough path in the transconductors is overcome by the provision in each of the transconductors (TC1 to TC4) of a non-reciprocal feedback capacitance ( $C_f$ ) which renders the feedthrough capacitance reciprocal thereby neutralising the feedthrough capacitance of the gyrator.

15 The devices include a filter (Figure 8, not shown) and a transceiver (Figure 10, not shown).

(Figure 7)

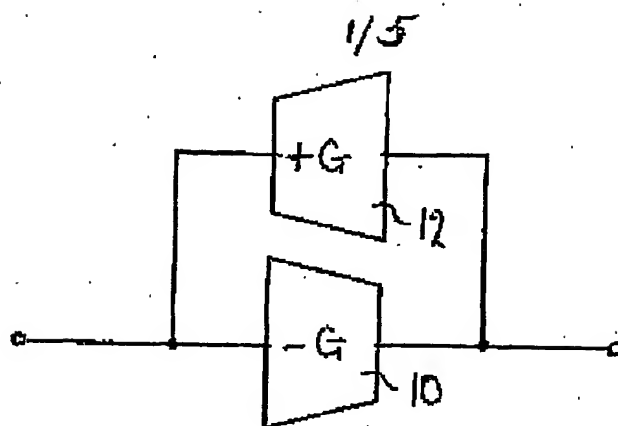


Fig. 1

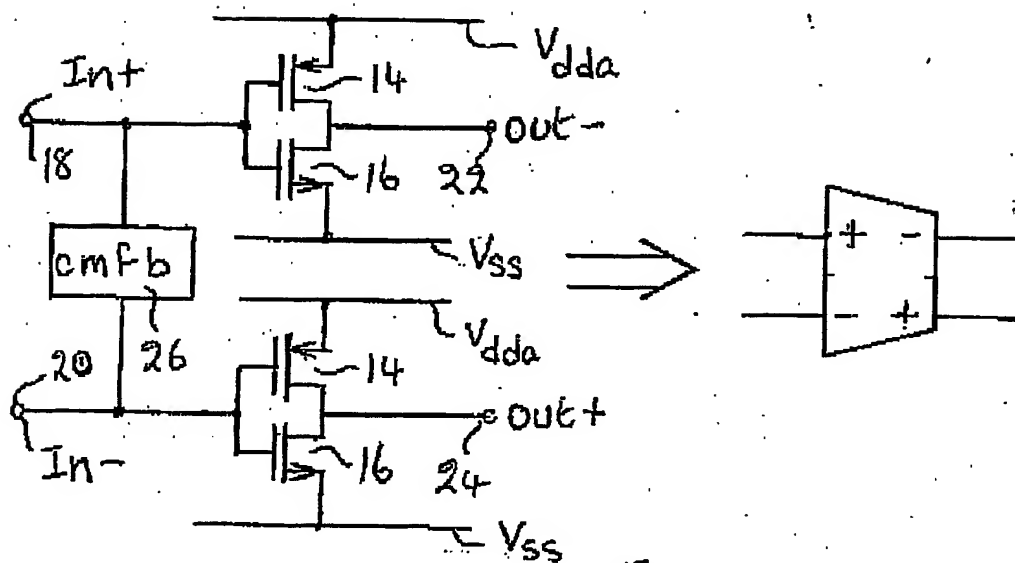


Fig. 2

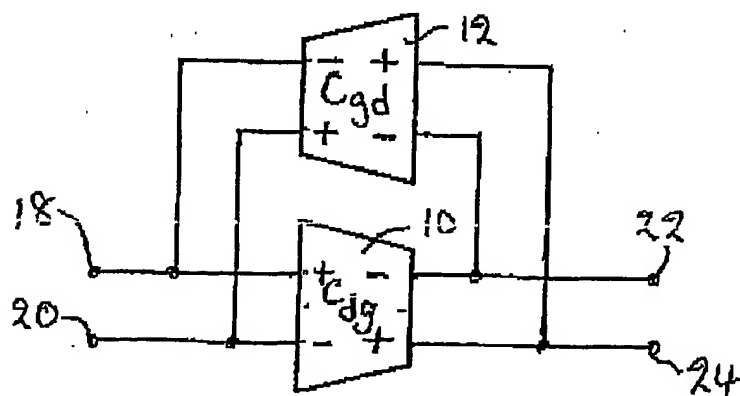


Fig. 3



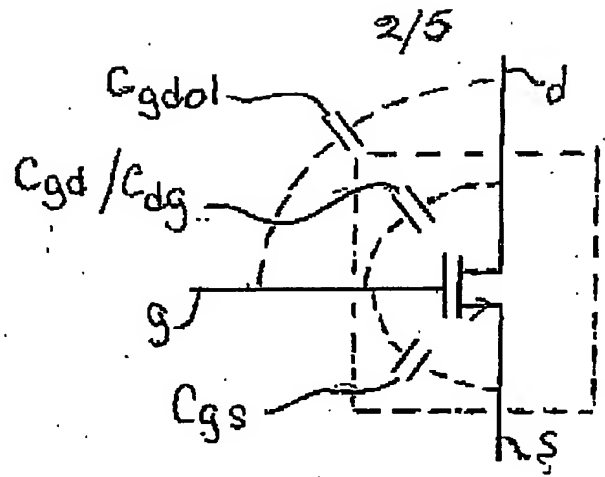


Fig. 4

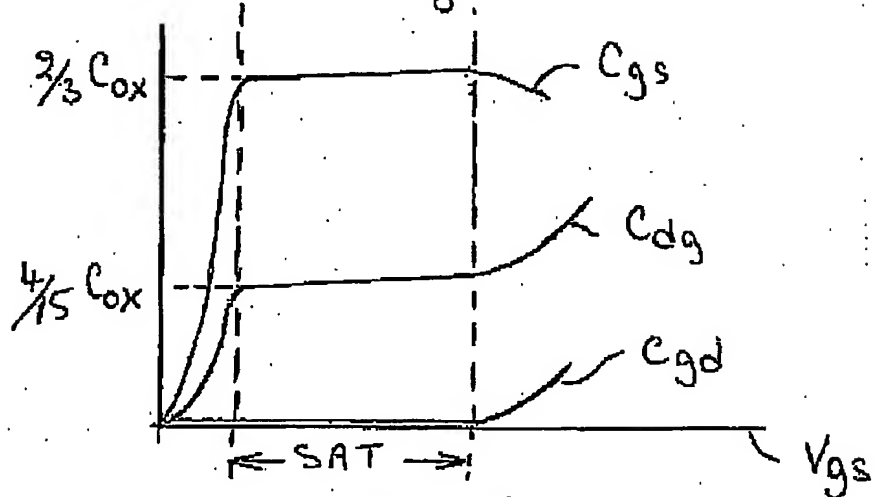


Fig. 5

3/5

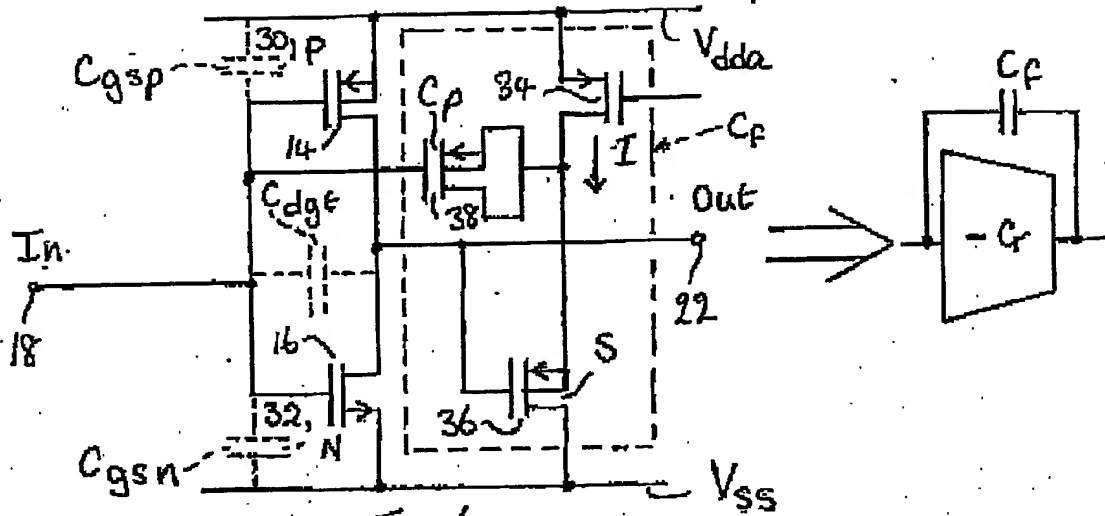


Fig. 6.

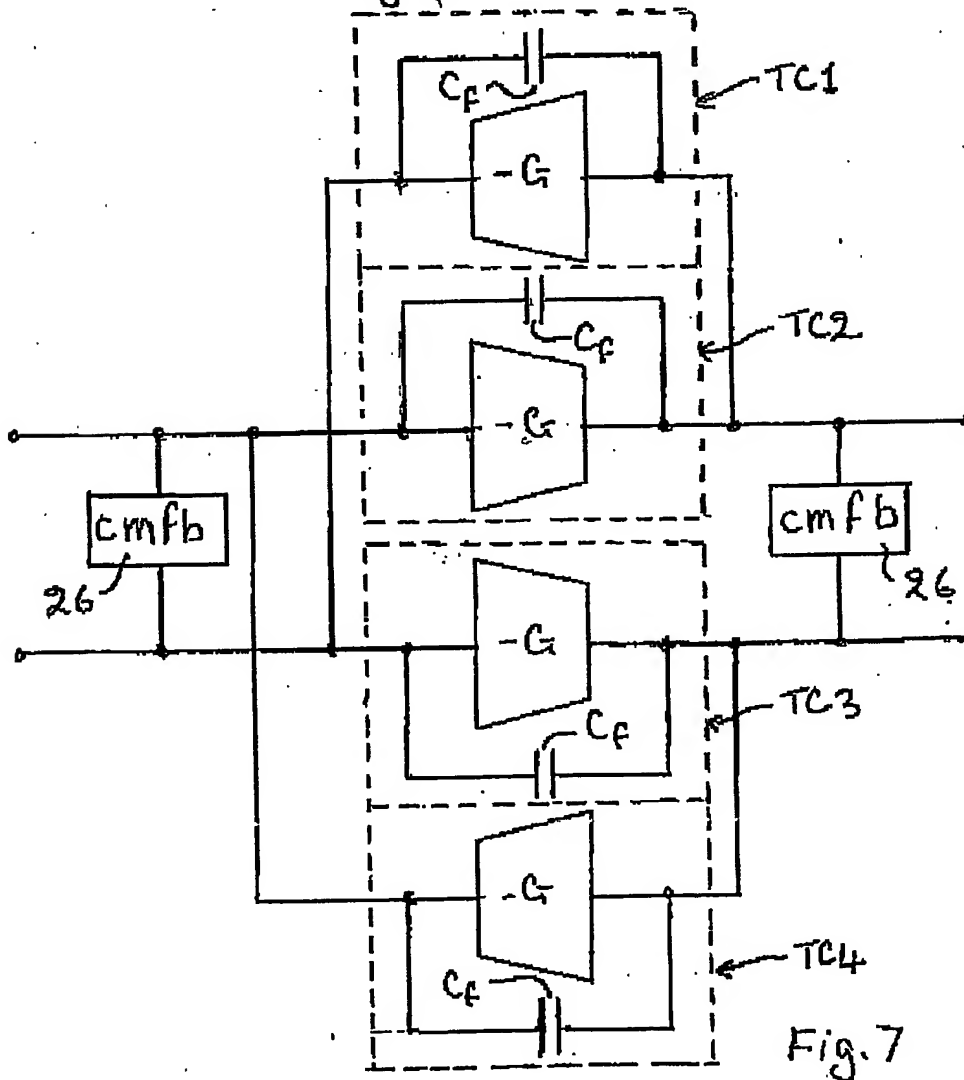
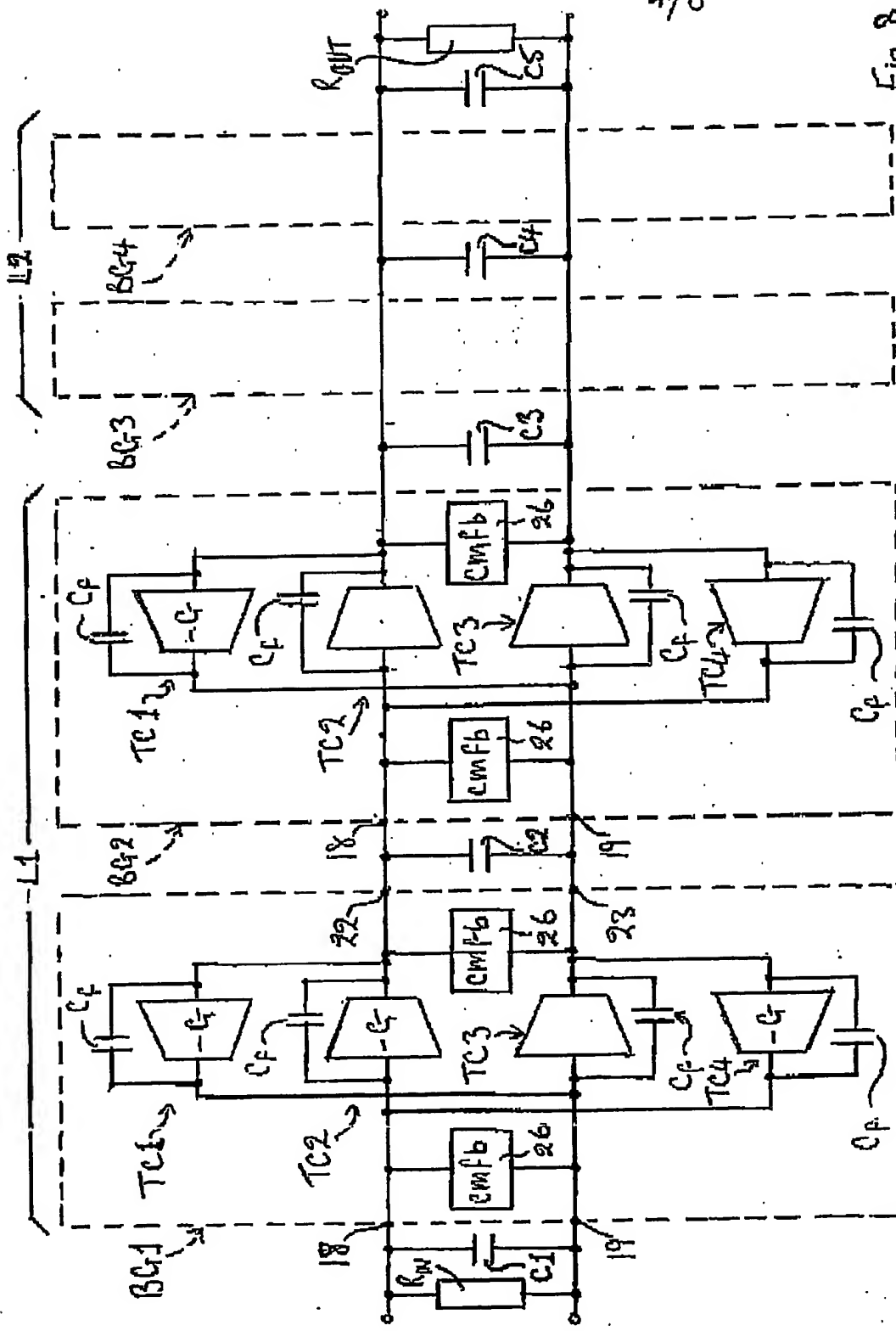


Fig. 7



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